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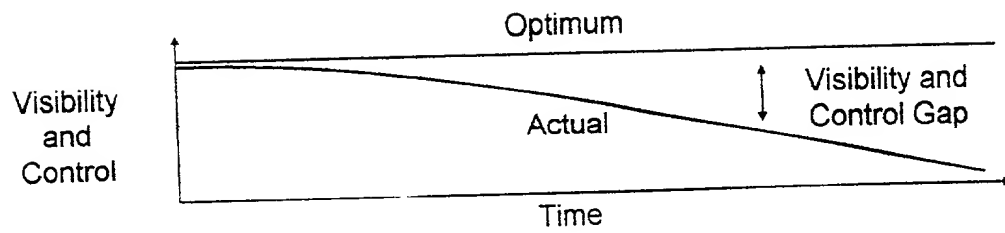


Figure 1 Visibility and Control Gap

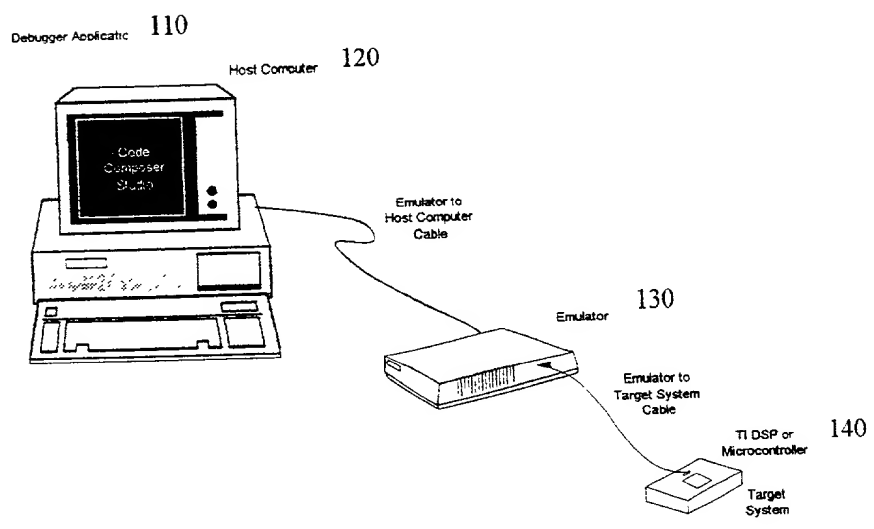


Figure 2 BeyondJTAG Emulation System

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140~

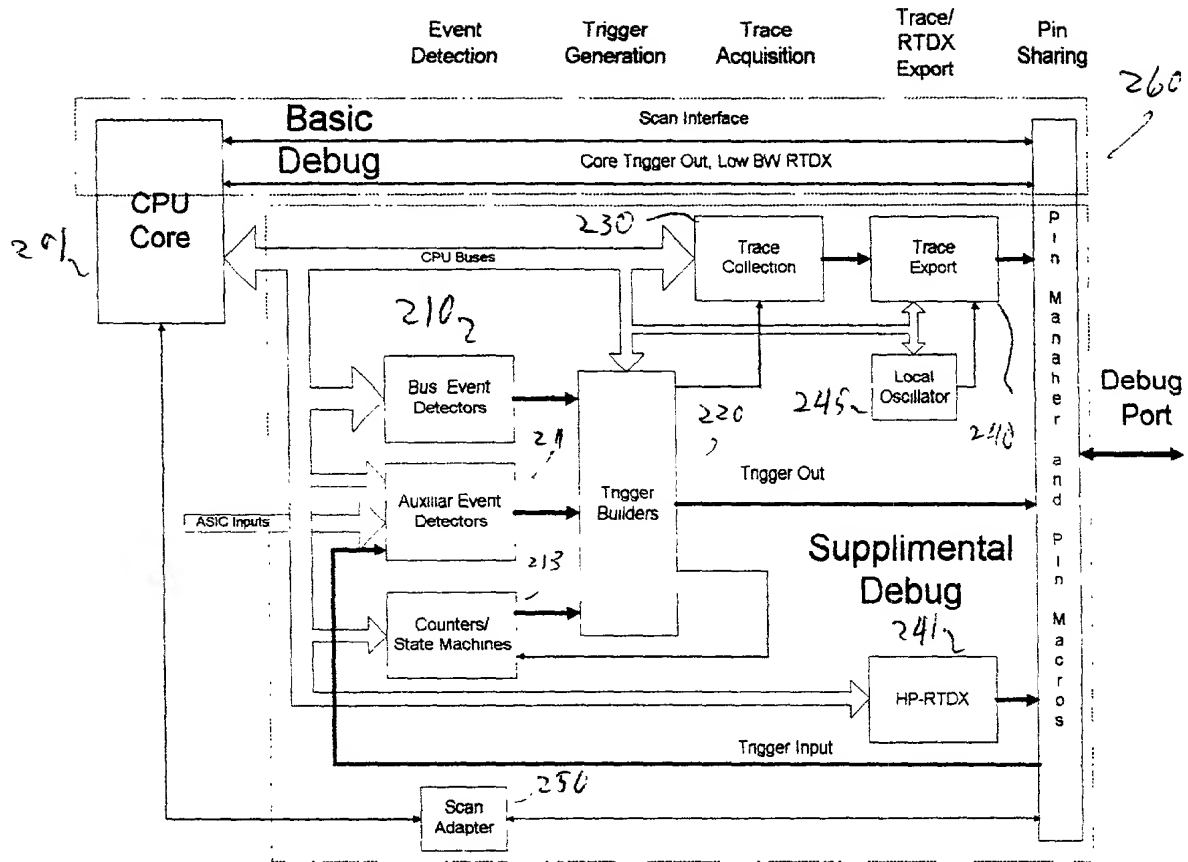


Figure 3 On-chip Debug Architecture

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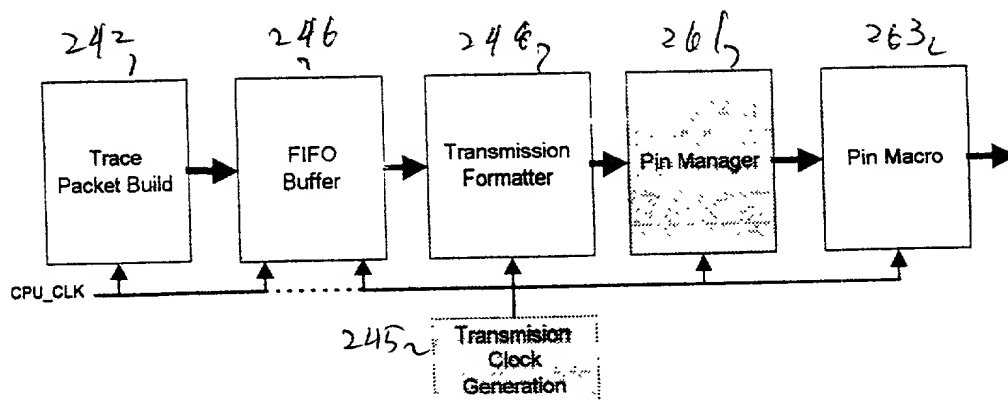


Figure 4 Trace Port Sections

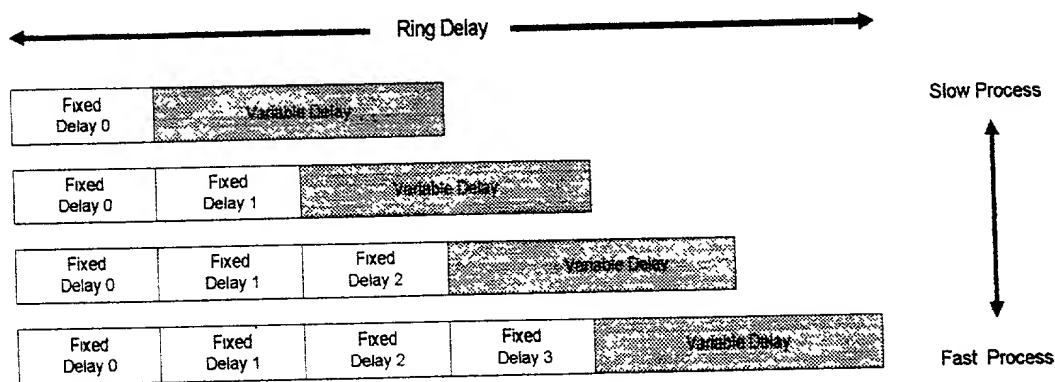


Figure 5 Ring Delay Options

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300

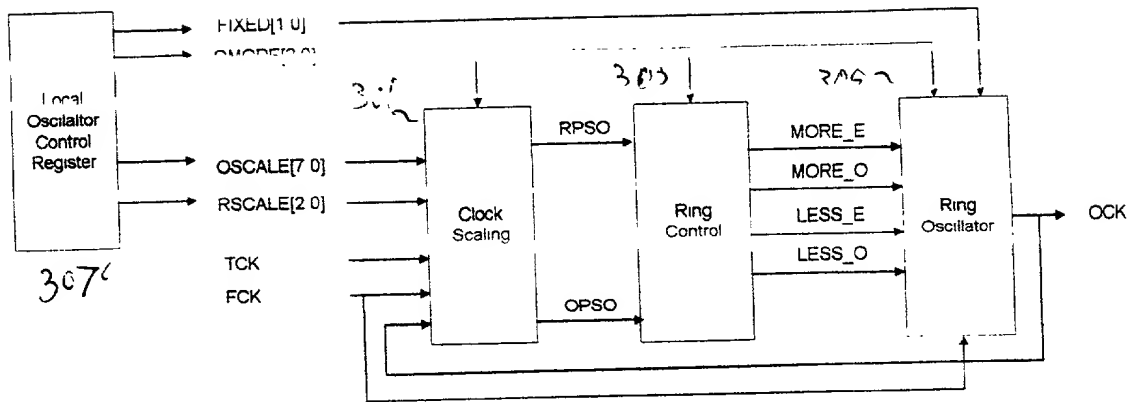


Figure 6 Local Oscillator

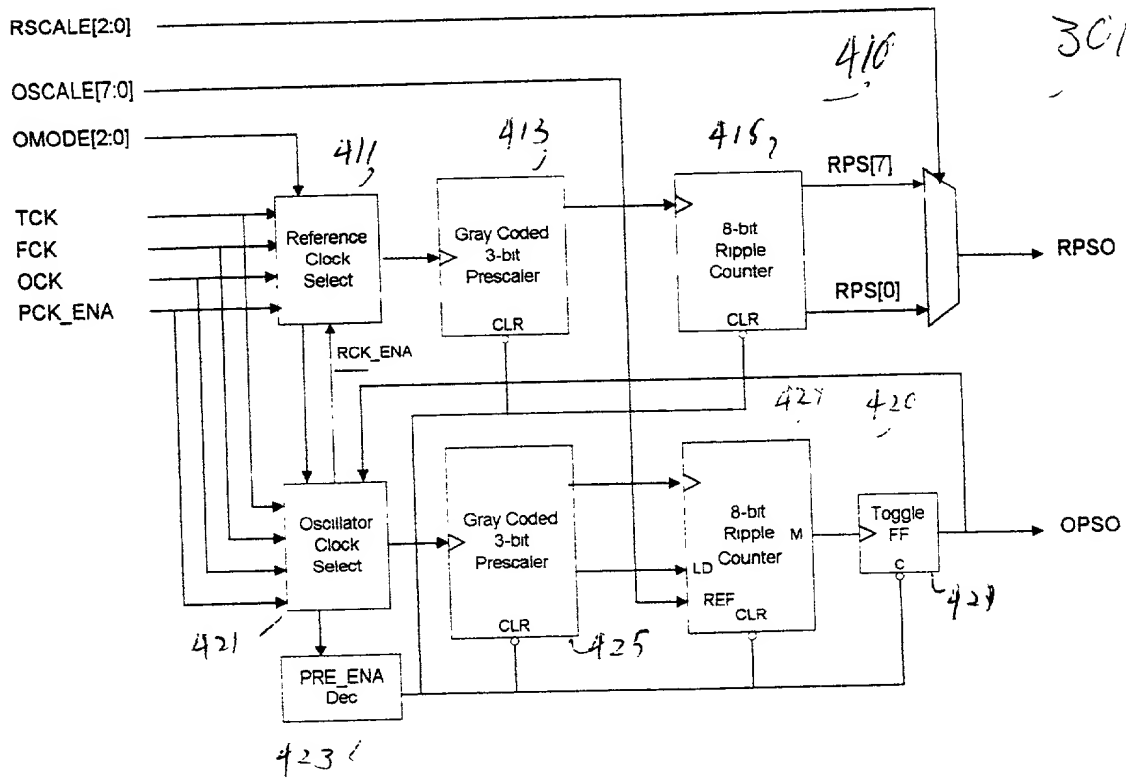


Figure 7 Clock Scaling Block

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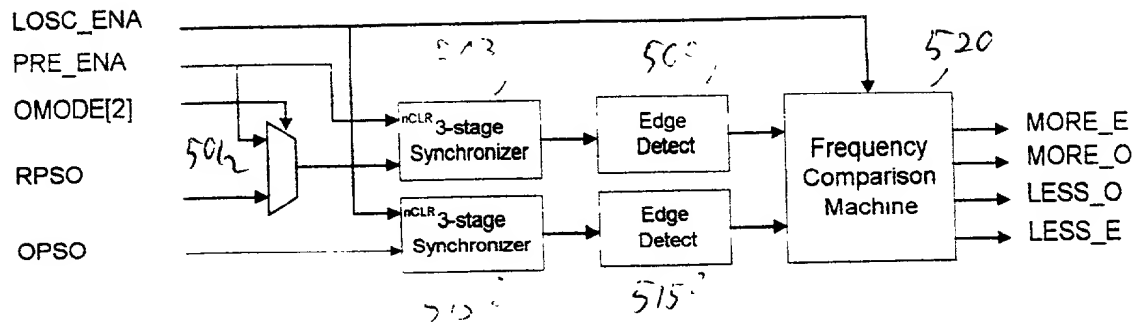


Figure 8 Ring Control Block

Signal Definition

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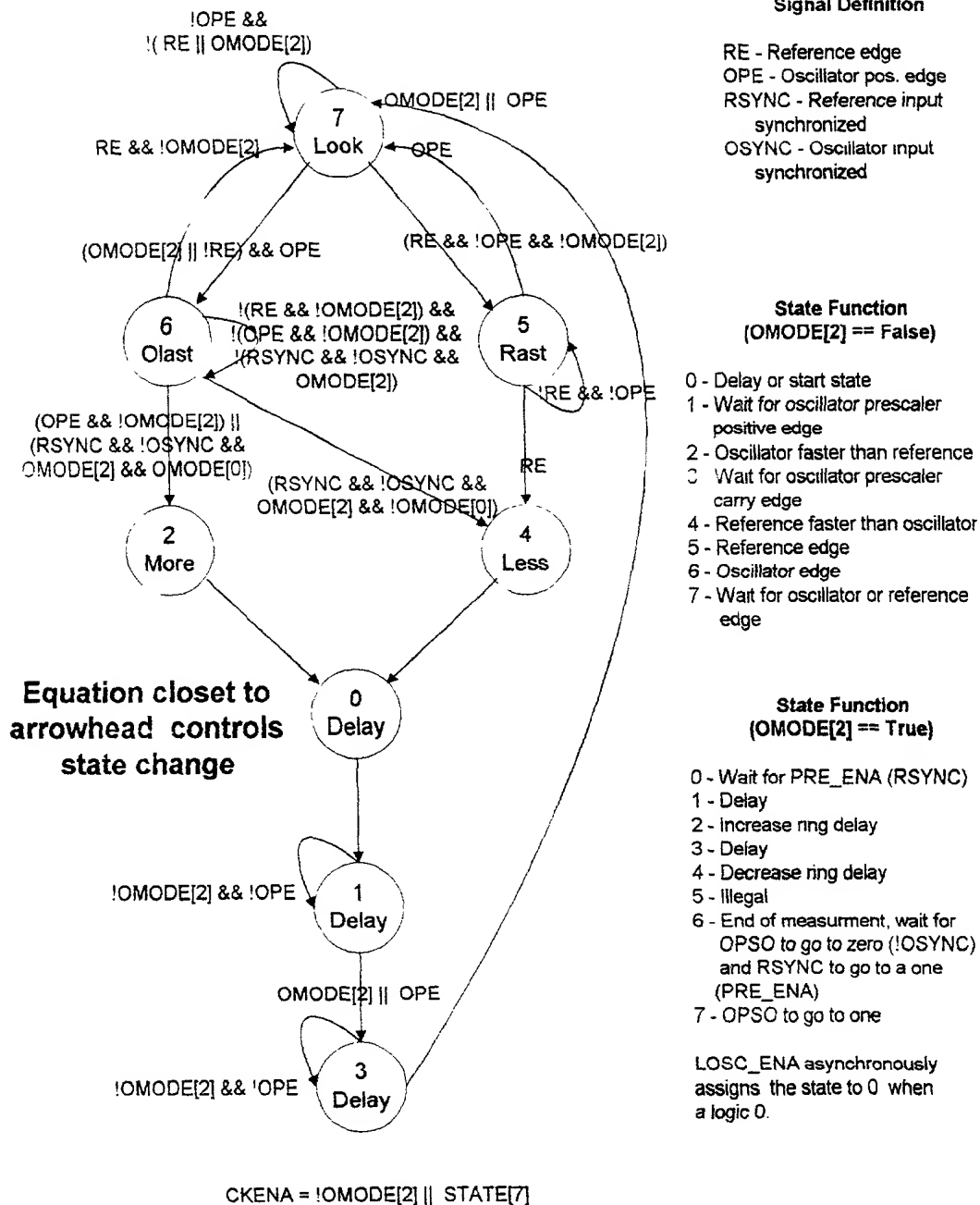


Figure 9 Frequency Comparison State Machine

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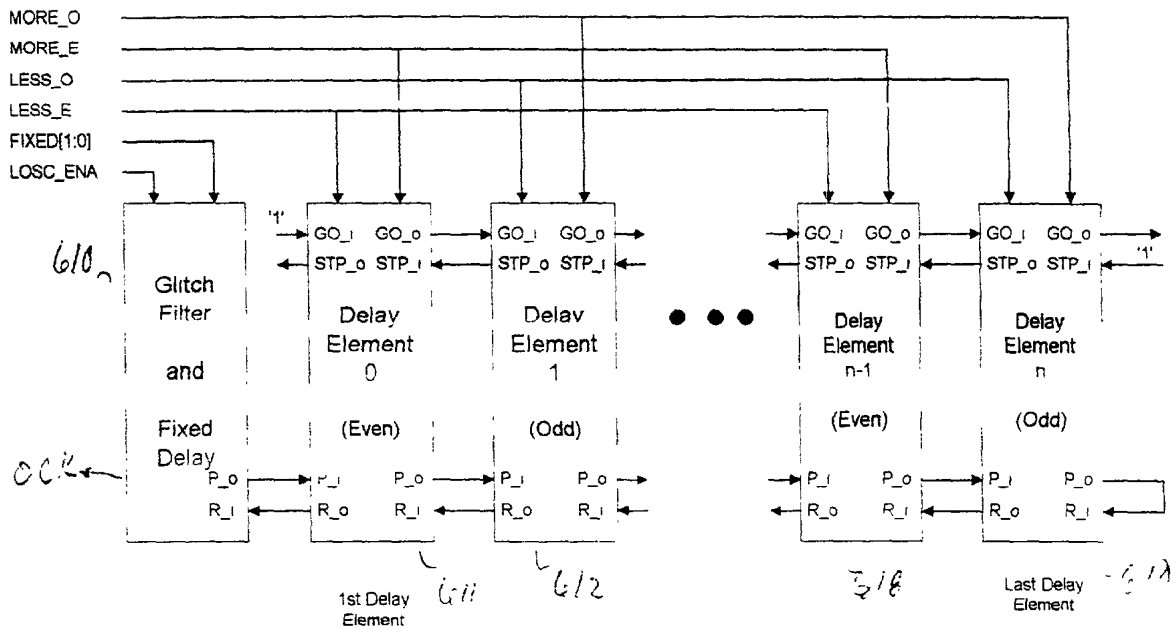


Figure 10 Ring Oscillator Block

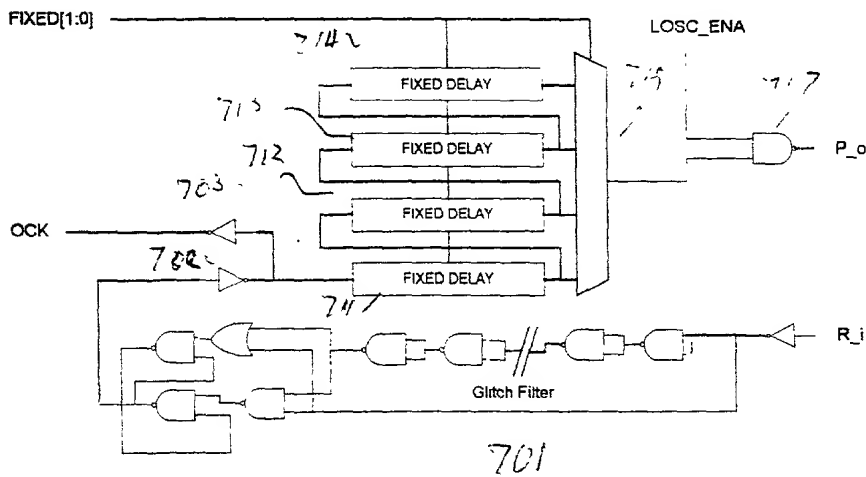


Figure 11 Glitch Filter and Fixed Delay

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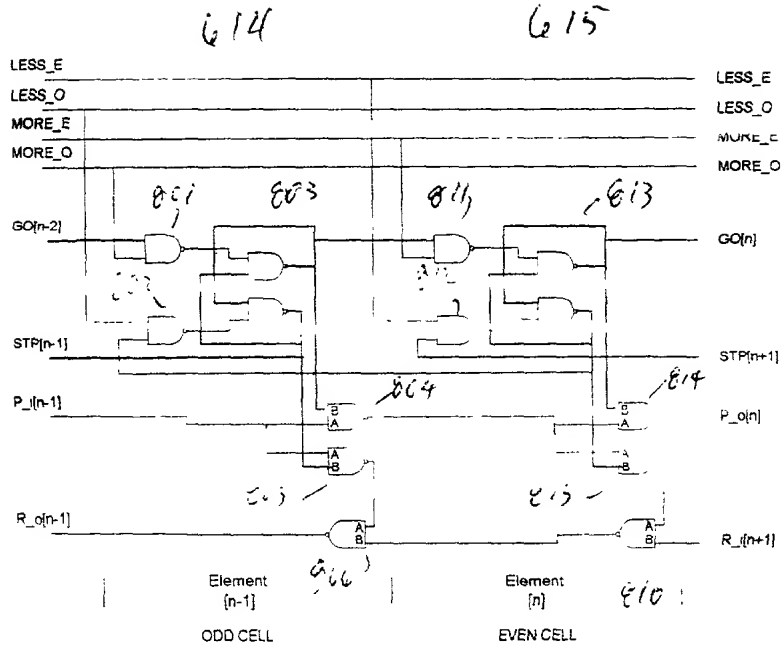


Figure 12 Even and Odd Delay Elements

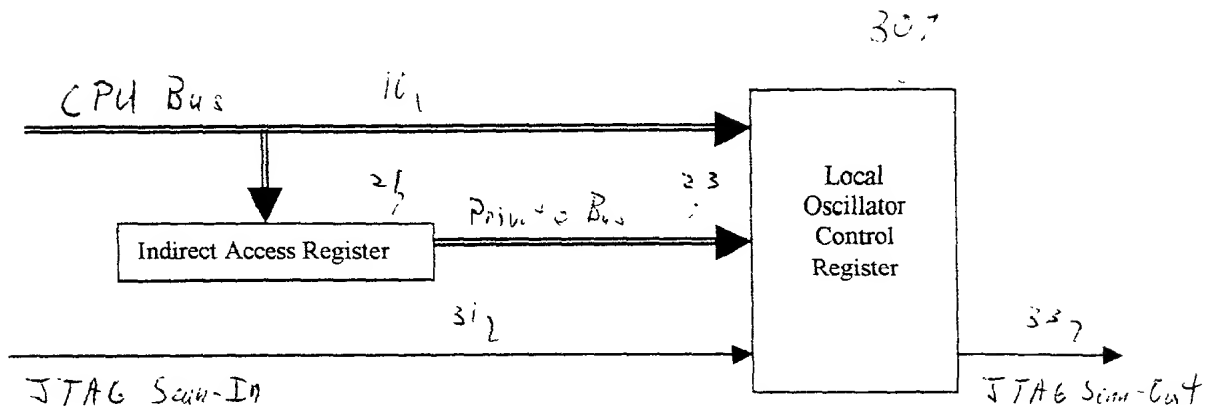


Figure 13